REMARKS

This is in response to the Office Action mailed on May 4, 2004, and the references cited therewith.

Claims 1, 3, 5, 6, 10, 14 and 15 are amended. Claims 2, 7 and 11-13, 17 and 19 are canceled. No new claims have been added; as a result, claims 1, 3-6, 8-10 and 14-16 and 18 are now pending in this application.

§103 Rejection of the Claims

Claims 1, 5, 6, 8-16 and 18 were rejected under 35 USC § 103(a) as being unpatentable over Huon et al. (U.S. Patent No.: 5,761,735) in view of Duffy (U.S. Patent No. 6,535,527) in further view of Santahuhta (EP 0989484).

Claims 2-4, 7, 17 and 19 were rejected under 35 USC § 103(a) as being unpatentable over Huon et al. (U.S. Patent No.: 5,761,735) in view of Duffy (U.S. Patent No. 6,535,527) in further view of Santahuhta (EP 0989484) as applied to claim 1 above, and further in view of Khandekar et al. (U.S. Patent No. 6,049,887).

Both Applicant and Huon describe circuits for synchronizing data transfers between a first and a second device operating at different data rates. In contrast to Huon, however, Applicant describes, and claims in claim 1-19, a system for performing this transfer synchronously. As can be seen in Huon at Figs. 1 and 2 , and as is described at col. 3, the memory device of Huon generates strobe signals. The strobe signals load appropriate registers and the registers are then read into a processor using the processor clock. The claims have been amended to emphasize the synchronous nature of Applicant's invention.

In addition, none of the cited references describe the use of secondary synch pulse as described by Applicant and claimed in claims 1, 3-6, 8-10 and 14-16 and 18 or the use of a hold pulse as described by Applicant and claimed in claims 6, 8-10 and 14-16 and 18.

As noted by the Examiner, Khandekar, like Applicant, describes a circuit for synchronizing data transfers between a first and a second device operating at different data rates when the clocks are both derived from a primary clock and repeat in a ratioed, systematic pattern.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

In addition, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143.

Although Khandekar, like Applicant, does describe a circuit for synchronizing data transfers between a first and a second device operating at different data rates when the clocks are both derived from a primary clock and repeat in a ratioed, systematic pattern, Khandekar solves the problem of transferring data between the two domains differently than does Applicant. In addition, there is no teaching or suggestion in Khandekar or in any of the other cited references to apply the approach described by Khandekar to the circuit described by Huon. Even if one did, the combined circuit would not look like the circuit described by Applicant and claimed in

claims 1, 3-6, 8-10 and 14-16 and 18. Reconsideration and issuance of a notice of allowance for claims 1, 3-6, 8-10 and 14-16 and 18 is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 4th day of November, 2004.

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